

Harvesting Wasted Heat in a Microprocessor Using Thermoelectric Generators: Modeling, Analysis and Measurement

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Abstract- Harvesting energy from previously unemployed ambient sources can play important role in saving energy and reducing the dependency to primary power sources (AC power or battery) of an electronic system. High-performance integrated circuits such as microprocessor, typically suffers from high surface temperature (in the order of 80-100°C) resulting from the high power density and limited cooling capacity of the package. In this paper, we consider the scope of harvesting thermoelectric energy from the wasted heat in a microprocessor leveraging on the temperature gradient between processor die surface and environment. First, we develop analytical model to accurately estimate the recycled energy considering the non-uniformity of temperature distribution in the die surface. Next, we analyze the effectiveness of the approach for thermoelectric generator (TEG) with different efficiencies (measured in terms of its figure of merit, ZT) under varying processor workload. Finally, we propose a possible arrangement for using the TEG on a processor and provide measurement results on the amount of harvested energy. The measurements on a Pentium III processor running at 1GHz show that we can harvest ~7mW of power from the processor for average workload using a commercial TEG.

I. INTRODUCTION

In today's world, depleting reserves of conventional energy sources such as fossil fuel and petroleum has forced mankind to seek for alternate sources of energy. New sources of energy such as solar energy, wind energy and hydropower etc. are being explored. However, an important alternate energy source that is often overlooked is thermal energy. Whenever, a work is done, small to large amounts of thermal energy is dissipated into air, which if converted back to electric energy may serve useful purpose. This paper will focus on the use of *Thermo Electric Generators* for converting wasted heat in high-performance integrated circuits such as microprocessor, into electric energy.

The foundation of thermal to electric energy conversion rests on the *Seebeck effect*, which involves the generation of an electromagnetic force (emf) when the two junctions of two dissimilar metal bars connected to each other are kept at different temperatures [1]. The structure consisting of dissimilar metals is often referred to as a thermoelectric generator (TEG). Researchers have already attempted to exploit this effect for conversion of electric energy from thermal energy. In [2], the authors have developed a semiconductor based TEG with P-N legs for energy conversion. The measurement results presented in [2] indicate energy conversion efficiency as high as 40%, by applying a temperature difference larger than 100°C. In [3], a TEG has been developed with an output voltage as high as 6.4V for a temperature level of 250°C-350°C at the hot side of the TEG.

These works demonstrate that thermoelectric conversion using a TEG is a promising energy harvesting application in future.

Modern high-performance chips operating at multi gigahertz frequency, such as microprocessors, consume large amounts of power (in the order of 40-100W) [20] and a substantial part of it is translated into heat. This heat creates a large temperature gradient between the die surface and environment. In order to ensure reliable operation of the die at elevated temperature, we need to design appropriate heat removal mechanism using high-efficiency heat spreader and heat-sink. A relevant question in this context would be: Can we exploit the thermal gradient in a high-performance chip to recycle the wasted heat energy into thermoelectricity using thermo electric generators?

In this paper, we have performed the modeling, analysis and measurement of the thermoelectric energy conversion in relation with a modern microprocessor and a commercial TEG. The electric energy continuously recovered from this wasted heat during the operation of the processor can be used to drive other components in a system or effectively stored for future use. Interestingly, the temperature distribution on the die surface is non-uniform (comprising of localized *hotspots* [17]) leading to a reduced thermoelectric conversion. The concept of using TEGs to generate electric energy from the wasted heat of a microprocessor was first proposed by Suski in a patent [4] and the feasibility was evaluated [5-6]. In this work, TEG was attached directly on the CPU and on the other side of the TEG a heat sink with cooling fan was attached.

Older thermoelectric generation devices typically used bi-metallic junctions, but most thermoelectric devices currently in use generate electricity utilizing semiconductor materials (such as Bismuth Telluride, Bi_2Te_3), which are good conductors of electricity, poor conductors of heat [12] and exhibit large values of Seebeck coefficient. These semiconductors are typically heavily doped to create an excess of electrons (n-type) or a deficiency of electrons (p-type). An n-type semiconductor will develop a negative charge on the cold side and a p-type semiconductor will develop a positive charge on the cold side, which forms a current flowing from one semiconductor leg to another. Since each P-N leg of a semiconductor thermoelectric device will produce only a few millivolts, it is useful to connect these legs in series to generate higher electric voltage. Researchers are also attempting to manufacture TEGs with high thermal conductivity, so that an integrated TEG can be an effective replacement for the heat spreader. However, due to limitations in the nature of the materials used for building the TEGs, the efficiency of the present-day TEG is less than 10% [13]. However, this recycled electric energy can be stored in a super-capacitor and reused later or can be used to drive low-power portable electronics such as MP3 players, or PDA, which can only consume about 110mW and 200mW, respectively [22].

The paper makes the following contributions:

- We have considered two scenarios for placement of a TEG on a processor for generating thermoelectric energy: 1) the TEG is directly integrated onto the substrate (for the best thermoelectric conversion efficiency) as shown in Fig. 1a; and 2) the TEG is integrated on top of the heat spreader as shown in Fig. 1b. For the first case, it is important to estimate the TEG efficiency as well as the resultant die thermal profile (affected due to presence of TEG in the heat-dissipation path) the considering the *non-uniform temperature distribution across the die surface*. We have developed analytical models to estimate the efficiency of the TEGs for the first case.

- Using the proposed model and an architecture-level thermal simulator (HotSpot [17]), we have analyzed the TEG efficiency as well as the temperature of the die surface for varying processor workloads. We have considered above two configurations for our analysis.

- We have presented measurement results from experiments performed with a commercial TEG and a Pentium III processor, in order to obtain a realistic estimate of the harnessed energy and determine the prospective applications of the recycled energy.

II. MODELING

Previous work presented in [6, 7] have tried to analyze the efficiency of a TEG which is directly attached to the CPU (Fig. 1a) or in a shunt setup (dashed box in Fig. 1b). In both cases, the surface of the TEG in contact with the CPU has been assumed to be at a constant temperature. However, in reality due to localized hotspots the die temperature is non-uniform and calculations based on the constant temperature profile will lead to inaccurate prediction of the TEG generated voltage.

A. TEG Efficiency Considering Non-uniform Temperature Distribution on Die Surface

At the steady state, the heat generated from the CPU is equal to the heat dissipated, so that the temperature of the CPU remains constant and the amount of heat received as input by the TEG can be considered to be a constant value. At this steady state condition, it is possible to model the TEG efficiency by determining the amount of heat that is converted into electric energy. Fig. 2 shows an operational model for the TEG, where the open circuit voltage is given by Equation (1).

$$U_o = N \cdot \alpha \cdot \Delta T \quad (1)$$

In Equation (1) U_o is the open circuit voltage, N is the number

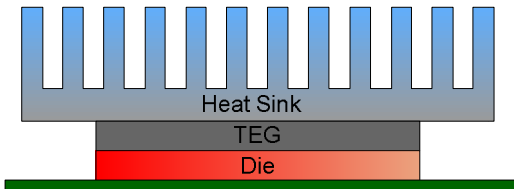


Figure 1a. TEG integrated on the die. It is placed between the package and the heat sink.

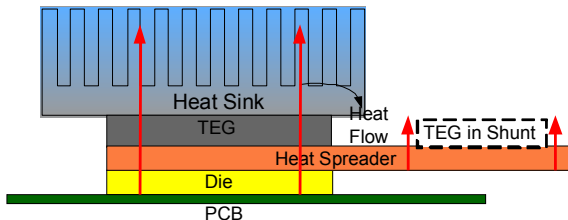


Figure 1 b. TEG integrated on the CPU. It is placed between the package and the heat sink.

of P/N leg pairs, α is Seebeck coefficient, ΔT is the temperature difference between two sides of the TEG. The power generated by the TEG is given by Equation (2).

$$P_L = I^2 \cdot R_L = \left(\frac{U_b}{R_L + R_{PN}} \right)^2 \cdot R_L = \left(\frac{N \cdot \alpha \cdot \Delta T}{R_L + R_{PN}} \right)^2 \cdot R_L = \left(\frac{N \cdot \alpha \cdot \Delta T}{R_L + \frac{2 \cdot N \cdot \rho \cdot L}{A}} \right)^2 \cdot R_L \quad (2)$$

In Equation (2), R_L is the load resistance, ρ is the density of the materials used to manufacture P/N legs, L is the length of one P/N leg and A is the cross-section area of one P/N leg. Under the condition of output load matching, the maximum power delivered by the TEG is given by Equation (3).

$$P_L = \left(\frac{N \cdot \alpha \cdot \Delta T}{R_{PN} + R_{PN}} \right)^2 \cdot R_{PN} = \frac{(N \cdot \alpha \cdot \Delta T)^2}{4 R_{PN}} \quad (3)$$

With above three basic equations, it is now possible to take into account the non-uniform temperature distribution at the hot side of the TEG in contact with the CPU.

We first partition the floorplan of the processor into number of different functional units such as integer unit, floating unit, cache, etc. If there are ' m ' partitions in total and unit m has an n_m P/N leg pair in contact with it, then the total open circuit voltage generated by the TEG can be represented as:

$$U_1 = n_1 \cdot \alpha \cdot \Delta T_1, U_2 = n_2 \cdot \alpha \cdot \Delta T_2, \dots, U_m = n_m \cdot \alpha \cdot \Delta T_m$$

The total voltage U_{Total} is:

$$\begin{aligned} U_{total} &= U_1 + U_2 + U_3 + \dots + U_n \\ &= n_1 \cdot \alpha \cdot \Delta T_1 + n_2 \cdot \alpha \cdot \Delta T_2 + \dots + n_m \cdot \alpha \cdot \Delta T_m \\ &= \alpha (n_1 \cdot \Delta T_1 + n_2 \cdot \Delta T_2 + \dots + n_m \cdot \Delta T_m) \end{aligned} \quad (4)$$

The total power generated by considering the non-uniform die temperature distribution can therefore be calculated as:

$$\begin{aligned} P_L &= \frac{U_{total}^2}{4 R_{PN}} \\ &= \frac{\alpha^2 (n_1 \cdot \Delta T_1 + n_2 \cdot \Delta T_2 + \dots + n_m \cdot \Delta T_m)^2}{4 R_{PN}} \\ &= \frac{\alpha^2 (n_1 \cdot \Delta T_1 + n_2 \cdot \Delta T_2 + \dots + n_m \cdot \Delta T_m)^2}{8 \frac{\rho \cdot L}{A} (n_1 + n_2 + n_3 + \dots + n_m)} \end{aligned} \quad (5)$$

$$\text{where, } R_{PN} = 2 \frac{\rho \cdot L}{A} (n_1 + n_2 + n_3 + \dots + n_m) \quad (6)$$

Thus given the number of P-N leg pairs per unit area and the area for each partition on the die floorplan, it is possible to accurately calculate the power generated from the TEG considering the non-uniform temperature distribution. A more practical configuration involving the generation of electricity from the wasted heat of the processor is shown in Fig. 1b, where the TEG is attached to the heat spreader layer. We will compare the effectiveness of energy recovery between the two

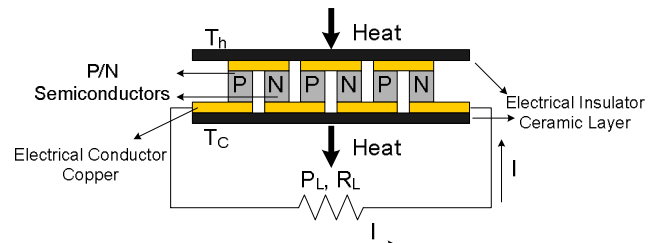


Figure 2. Operating model for a TEG. The semiconducting P/N legs (connected in series) generate electricity due to thermal gradient.

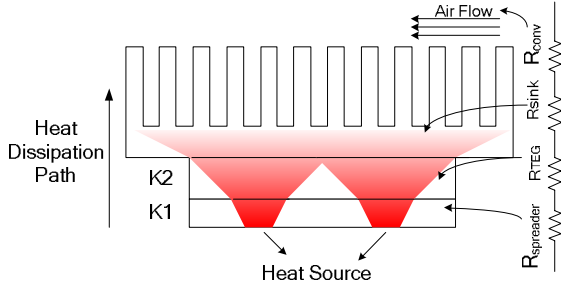


Figure 3. Heat conduction and spreading paths from inside the chip to the ambient. configurations in Section III.

B. Die Thermal Profile with Integrated TEGs

In both cases, it is important to calculate the die temperature profile in presence of the TEG. The primary reason is that due to the low thermal conductivity of the TEG, the thermal resistance in the heat dissipation path increases, which results in less amount of heat being dissipated to the environment in unit time leading to an increase in the die temperature. The steady-state thermal profile of the die will depend on the TEG material and heat load from the processor.

The previous work presented in [8-11] which model the heat conduction and spreading within the package constitute the basis of our estimation of the die thermal profile in presence of the TEG. Inside the package of the chip, a three-dimensional heat flow exists from the device layer to the ambient. Fig. 3 shows the heat dissipation path from inside the chip to the ambient, and Fig. 4 shows the equivalent thermal resistance network along which the heat dissipates. As seen from Fig. 3, the heat suffers refraction when it moves from a layer with thermal conductivity k_1 to k_2 , the angle of refraction θ is given by Equation (7) [8].

$$\theta = \tan^{-1} \left(\frac{k_1}{k_2} \right) \quad (7)$$

Since each layer inside the package behaves as a heat source for the layer above it, we calculate the thermal resistance of the TEG using the formula for thermal resistance presented in [9], which takes into account the two-dimensional spreading of heat. The resistance as given by Equation (8) considers x and y to be the length and width of the heat source, and L and k to be thickness and the thermal conductivity of the layer in contact with the heat source.

$$R = \frac{1}{2k \tan \theta (x-y)} \cdot \ln \frac{y + 2L \tan \theta}{x + 2L \tan \theta} \cdot \frac{x}{y} \quad (8)$$

The total thermal resistance along the heat dissipation path as shown in Fig. 3 and 4 is the summation of the thermal resistance of each component. For example, when the TEG is attached to the heat spreader, the total thermal resistance is represented by Equation 9, where $R_{substrate}$, $R_{spreader}$, R_{TEG} , R_{sink} and R_{conv} are the thermal resistances of substrate, heat spreader, TEG, heat sink and convection, respectively.

$$R = R_{substrate} + R_{spreader} + R_{TEG} + R_{sink} + R_{conv}. \quad (9)$$

$R_{substrate}$, $R_{spreader}$, and R_{TEG} can be calculated by using equations 7 and 8. For $R_{substrate}$, the area of the heat source is equal to the area of each functional block and the spreading angle can be determined by the thermal conductivity ratio of the heat spreader and silicon substrate. The thermal resistance of the heat spreader and TEG can be estimated using the same

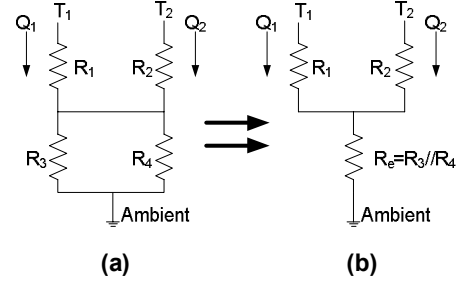


Figure 4. Equivalent resistance network for Fig. 3.

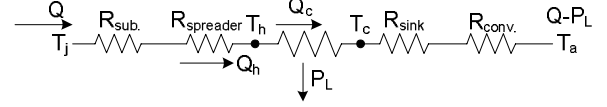


Figure 5. Thermal resistance network of the heat flow from inside the chip to the ambient with TEG attached to the CPU.

method. However, the area of the heat source for heat spreader and TEG is the original heat source area plus an area expansion due to heat spreading as shown in Fig. 3. For heat spreader, the length and width of the heat source is:

$$(x + 2L_{substrate} \tan \theta_{substrate}) (y + 2L_{substrate} \tan \theta_{substrate})$$

For TEG, the length and width of the heat source is:

$$(x + 2L_{substrate} \tan \theta_{substrate} + 2L_{spreader} \tan \theta_{spreader})$$

$$(y + 2L_{substrate} \tan \theta_{substrate} + 2L_{spreader} \tan \theta_{spreader})$$

Here, the spreading angle is related to the thermal conductivity of the heat spreader and substrate [8].

Due to the spreading effect in the intermediate layers, every section of the heat sink receives the same amount of heat and therefore it suffices to calculate the total resistance of the heat sink, instead of sections on top of each functional unit. The thermal resistance of the heat convection is given by Equation (10), where h is the heat convection coefficient and A is the effective area of the heat sink. The method for calculating effective area of the heat with straight fins is described in [12].

$$R_{conv} = \frac{1}{h \cdot A} \quad (10)$$

From Fig. 3, we find that the heat dissipation paths merge after a point. This phenomenon indicates that the steady-state temperature of the layers, which are along the heat dissipation path but are away from the die surface, will depend on the power consumption of all on-chip heat sources as given by Equation 11.

$$T(x, y) = \sum_{i=1}^N R_i \cdot Q_i \quad (11)$$

In Equation 11, $T(x, y)$ is the temperature at location (x, y) on the surface of an intermediate layer, which may be either heat spreader or the TEG. R_i is the thermal resistance between heat source i and location (x, y) . Q_i is the power consumption of heat source i , N is the total number of on-chip heat sources. From Fig. 3, we can also derive an equivalent thermal resistance network as shown in Fig. 4. In Fig. 4, Q_1 and Q_2 are the heat generated by two heat sources. T_1 and T_2 are the temperature of two heat sources. The heat dissipation paths for these two heat sources are initially separated but will merge finally due to heat spreading. Due to heat spreading, temperature of the surface of an intermediate layer will be uniform, which is indicated by the equivalent parallel resistor

R_c in Fig. 4b. The distance at which heat from different source merge together can be estimated based on the heat spreading angle in each packaging layer and the distance between each heat sources. The junction temperature T_1 and T_2 can be estimated as:

$$T_1 = Q_1 R_1 + (Q_1 + Q_2) R_c \quad (12)$$

$$T_2 = Q_2 R_2 + (Q_1 + Q_2) R_c$$

Hence, the general term of the equation for calculating junction temperature by considering inter-heat source correlation can be estimated as:

$$T_i = Q_i R_i + (Q_1 + Q_2 + Q_3 + \dots + Q_n) R_c \quad (13)$$

$$R_c = R_1 // R_2 // R_2 // \dots // R_n$$

Where T_i is the junction temperature of i^{th} heat source, Q_i and R_i are the heat generated by the i^{th} heat source and the thermal resistance along the heat dissipation path for the i^{th} heat source before the heat from different sources merge together. Thus, based on Equation (8), it is possible to calculate the thermal resistance of each intermediate layer. Equation (13) provides the temperature of the heat sources on the die after the TEG is attached to the heat spreader. The equivalent thermal resistance network corresponding to the heat flow from inside the chip to the ambient is shown in Fig. 5.

III. ANALYSIS

In this section, we will analyze two possible

configurations discussed in Section II in terms of their effectiveness of energy conversion. One is to attach the TEG to substrate (Fig. 1a) and the other is to attach the TEG to the heat spreader (Fig. 1b). Before we analyze the configurations, it is necessary to define a figure of merit for the TEG, a higher value of which translates to a higher TEG efficiency. Such a merit (referred as “ ZT ”) as defined in Equation (14) indicates that good thermoelectric materials should have large Seebeck coefficient α , higher electrical conductivity σ , higher hot side temperature T_h , and low thermal conductivity λ and can therefore achieve higher efficiency for thermoelectric conversion.

$$ZT = \frac{\alpha^2 \sigma}{\lambda} T_h \quad (14)$$

A. TEGs Attached to Substrate

In this subsection, we have analyzed the effect of attaching the TEG directly to the silicon substrate of the chip (Fig. 1a). Since the dimensions of the TEG are taken to be same as that of the die, it has fewer P-N leg pairs compared to the case where the TEG is attached to the heat spreader. According to the thermal resistance models developed in the previous section, we have calculated the temperature distribution of the substrate after attaching the TEG. Power trace files for an Alpha 21264 microprocessor were obtained by simulating different SPEC95 benchmarks on Wattach

Table I. Recovered power and the temperature of the hottest spot on the substrate after attaching the TEG on top of the substrate. Two types of TEG (corresponding to two TEG materials with $ZT=1$ and $ZT=2$) are considered.

SPEC-95 Benchmark	Recycled power (mW)		Initial temperature	Final temperature of the hot spot	
	ZT=1	ZT=2		ZT=1	ZT=2
APPLU	132	369	135.12°C	127.37°C	168.84°C
APSI	55	153	101.85°C	96.20°C	122.82°C
CC1	77	214	114.68°C	106.71°C	138.22°C
Compress95	80	224	95.58°C	92.26°C	117.04°C
Go	123	344	138.92°C	125.18°C	165.23°C
hydro2d	111	311	126.98°C	120.11°C	158.15°C
Li	102	285	123.95°C	116.74°C	153.14°C
M88ksim	126	352	133.25°C	125.40°C	165.88°C
Perl	109	304	127.41°C	119.81°C	157.43°C
turb3d	124	345	132.20°C	124.49°C	164.58°C
wave5	106	295	124.90°C	118.17°C	155.12°C

Table II. Recovered power and the temperature of the heat spreader after attaching the TEG on the heat spreader. Two types of TEG (corresponding to two TEG materials with $ZT=1$ and $ZT=2$) are considered.

SPEC-95 Benchmark	Recycled power (mW)		Initial temperature	Final temperature of the spreader	
	ZT=1	ZT=2		ZT=1	ZT=2
APPLU	26	76	44.33°C	64.53°C	76.25°C
APSI	11	31	42.67°C	55.74°C	63.27°C
CC1	15	44	42.77°C	58.64°C	67.55°C
Compress95	9	27	42.36°C	54.65°C	61.67°C
Go	24	71	43.99°C	63.68°C	75.01°C
hydro2d	22	64	43.97°C	62.50°C	73.25°C
li	20	59	43.87°C	61.52°C	71.82°C
M88ksim	25	73	44.01°C	63.94°C	75.39°C
perl	21	63	43.92°C	62.25°C	72.88°C
turb3d	24	71	44.02°C	63.71°C	75.04°C
wave5	21	61	43.91°C	62.15°C	72.39°C

architecture level performance and power simulator (version 1.0) [21]. Using the power trace information for each functional block of the processor and Equations 7-13, it is possible to estimate the junction temperature of each functional block. For calculating the power and the temperature, a few assumptions were made about the dimensions of the die and the TEG. Because power trace is obtained from an Alpha 21264 microprocessor, we use the dimensions of this microprocessor for simulation [17]. The dimension of the die (as well as of the TEG) is taken to be $18\text{mm} \times 18\text{mm}$ with a 0.5mm thickness. The dimension of the heat sink is assumed to be $60\text{mm} \times 60\text{mm}$ with a 6.9mm thickness. The height and width of the P-N leg is assumed to be 1mm and 0.5mm , respectively. With this dimensional data, it is now possible to calculate the number of P-N legs that are in contact with each functional block. Other parameters like Seebeck coefficient (α), thermal conductivity of TEG (λ) and its electrical resistivity were obtained from [6], where the reported value for ZT is 0.9. Calculations have also been made on the basis of the parameters presented in [22], where a value of $ZT=2$ has been reported. Table I reports the power generated by the TEG and the highest junction temperature on the die after attaching the TEG to the substrate for $ZT=1$ and $ZT=2$, respectively.

For $ZT=1$ in Table I, we see that the highest junction temperature decreases after the TEG is attached to the substrate. Such a fall in temperature can be attributed to the fact that the thermal conductivity of the TEG is very low, about 100 times lower than that of the substrate. As we had mentioned previously, heat suffers a refraction when it moves from one medium to another. The refraction angle is related to the thermal conductivities of two mediums. Due to the large difference in the thermal conductivity of these two media, the heat refraction angle is very large, so that the heat generated by each functional block of the microprocessor will spread to the entire TEG, which suggests a uniform temperature distribution on the TEG. Due to high thermal resistance of TEG, the non-uniform temperature distribution of the die is also alleviated because the large amount of heat generated by the localized hotspot can be transferred to the cooler region on the die through the TEG. In spite of this heat transfer, the temperature of the cooler region remains almost constant due to its large area compared to the hotspots. For the *APPLU* benchmark, the temperature difference between the hotspot and the cool region is only about 10°C before the TEG is attached to the substrate, which is almost same as the decrease in the temperature of the hottest spot on the substrate.

For a TEG with $ZT = 2$, the thermal conductivity of the TEG material is much lower compared to a material corresponding to $ZT = 1$. In this case, due to the very high thermal resistance of the TEG, the amount of heat that can be transferred through the TEG is significantly reduced. Thus the temperature of the hottest region of the substrate substantially increases (Table I) after the TEG is attached to the substrate.

B. TEGs Attached to Heat Spreader

In this scenario, the TEG is attached on the heat spreader, which has a larger area than the die. The dimension of the TEG is taken to be same as that of the heat spreader, i.e. $30\text{mm} \times 30\text{mm}$ with a thickness of 1mm . The dimensions of the die and heat sink are same as in the previous case. Calculations were performed for both $ZT=1$ and $ZT=2$. Other parameters of the TEG such as Seebeck coefficient, thermal conductivity, electrical resistivity etc. were kept unchanged. The output

power and the temperature of the heat spreader are provided in

From Table II, we can see that the power generated by the TEG decreases when attaching the TEG on the heat spreader. In this scenario, the TEG is attached to the heat spreader, so the temperature at the hot side of the TEG decreases compared to the previous scenario, and if the ambient temperature is kept constant, the temperature gradient across the TEG reduces. Although the number of P/N legs increases due to an increase in the area of the TEG, temperature gradient across the TEG reduces significantly. This cannot be compensated by the increase in the number of P-N legs. Compared to the heat spreader, the thermal resistance of the TEG is quite large, which translates into an additional large thermal resistance between the heat spreader and heat sink. This reduces the heat transfer rate from the heat spreader to the ambience, resulting in an increase in temperature of the heat spreader (Table II).

IV. MEASUREMENT RESULTS AND APPLICATIONS

A. Measurement Results

In order to find out the amount of energy harnessed from the wasted heat of a microprocessor, experiments were carried out to determine the range of power generated by a commercial TEG in a practical scenario. The experimental setup consisted of an Intel Pentium III processor running Windows XP system applications (no user applications) at 1GHz with the heat sink and cooling fan removed. A thin copper plate (used as heat spreader) was attached on the package of the CPU by using a thermal gel in order to make a good thermal contact between the CPU and the copper plate. A Bi-Te based commercial TEG [18] was then attached on the copper plate. Fig. 6 shows our experimental setup. The CPU lying beneath the copper plate is depicted by a red bulge on the Cu plate. The TEG rests on the other end of the Cu-plate, which forms a shunt for the heat to be transferred from the CPU to the TEG. The shunt method (which is shown as a dashed box in Fig 1a) can provide an additional parallel heat dissipation path, compared to directly attaching the TEG above the CPU.

The experiments were then carried out for four different scenarios which are as follows: 1) the Cu plate rests on the CPU and the TEG rests on the Cu shunt away from the CPU, both Cu plate and the TEG being exposed to the ambience. 2) The position of the TEG is same as before, except that the surface of the TEG not in contact with the Cu plate is kept in contact with a cooler surface. This allows a higher temperature gradient across the TEG, allowing higher energy conversion compared to scenario I. 3) The Cu-plate still rests on the CPU and TEG is attached on the section of the Cu-plate which is exactly above the CPU, and the TEG is exposed to the ambience. 4) The configuration is similar to scenario III, except that the upper surface of the TEG is cooled using a cold surface to increase the thermal gradient.

Table III presents the power and temperature values obtained from our measurements for the four cases discussed above. In order to verify the correctness of our measurement, we have also calculated the expected values of the generated power based on the specifications of the commercial TEG. On an average, we find the measured power values are lower by about 20% compared to the expected ones. The discrepancy between the measured and the expected values can be attributed to the fact that we have only measured the temperature difference between the bottom layer and the top

Table III. Measurement results of energy recycled and the temperature of the CPU and TEG.

Test condition		Temp. of CPU	Temp. of Cu plate	Temp. of TEG	Voltage	Current	Impedance matched power
TEG on shunt	Scenario I	77°C	43°C	40°C	87.7mV	14.5mA	0.3 mw
	Scenario II	77°C	43°C	37°C	200.1mV	30.1mA	1.5 mw
TEG on CPU	Scenario III	77°C	59°C	53°C	210.3mV	31.6mA	1.7 mw
	Scenario IV	77°C	59°C	47°C	418.8mv	64.3mA	6.7 mw

ceramic layer of the TEG, which is not indicative of the actual temperature difference that exists between the two metal junctions. In reality, the temperature difference will be lower than the measured value. Moreover, the estimated power value assumes a perfect thermal contact between Cu plate and the TEG, which is difficult to achieve in the experimental setup. The amount of recycled power depends on 1) the TEG efficiency and 2) temperature of the cooler side of the TEG. Scenario II and IV support that if there is cooling in the open side of TEG, more power can be recycled. Note that, the maximum conversion efficiency is determined by the Carnot efficiency, which is about 4% assuming a temperature difference of 12°C and a high temperature of 59°C.

B. Application to an Electro-Osmosis System

Although the recycled energy is only several mW (as shown in Table III), high-efficiency TEG materials can be used to increase the recycled energy considerably. Recently, different thermoelectric modules based on novel materials and structures (such as superlattice systems) and their potential applications have been reported [14-15]. In [15], the authors have developed a TEG with a maximum thermoelectric conversion efficiency of 5.6%, which was applied to collect the wasted heat from a bulb in a projector system and operate cooling fans and other electronic devices.

A possible way to reuse the harvested thermoelectricity is to drive an *electro-osmosis system* to cool the CPU. Electro-osmosis, [16], is being considered as an efficient cooling mechanism for modern microprocessors. For an electro-osmosis system, based on dimensions, the driving voltage may vary from mV to several volts. Based on specification of the microprocessor system, it is, therefore, possible to design an electro-osmosis system that operates at low voltage and power supplied by the TEG.

V. CONCLUSION

In this paper, we have presented a model to accurately

estimate the TEG efficiency by considering the non-uniform temperature distribution on the die surface. Models to estimate the final temperature of the die surface after attaching the TEG to the substrate are also presented. Using our model, we have analyzed the TEG efficiency and die temperature for different processor workloads. Finally, experiments were carried out to measure the power that can be generated by a commercial TEG in a realistic scenario, and suggest potential applications for such thermoelectric systems.

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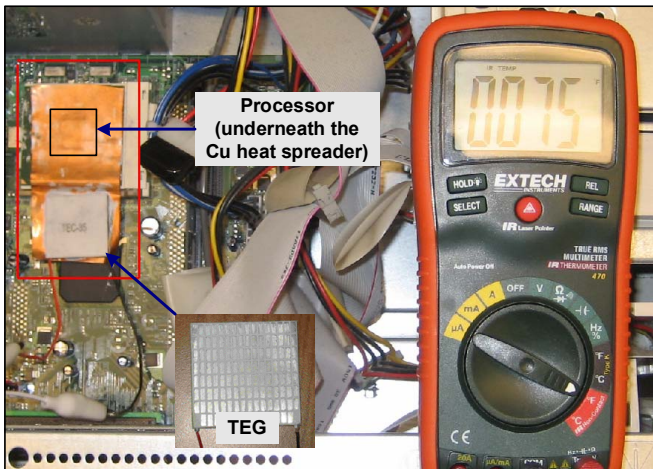


Figure 6. Measurement setup with a Pentium III processor and a commercial TEG.